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ABSTRACT OF THE DISCLOSURE

A semiconductor die assembly employing a voltage reference plane structure electrically isolated from, but in immediate proximity to, leads of a lead frame to which the die is electrically connected. A non-conductive adhesive or an adhesively-coated dielectric film is used to position the voltage reference plane on the leads. The voltage reference plane is electrically connected to a ground or other reference potential pin of the die through a connection to one of the leads. The assembly is encapsulated, preferably by transfer-molding of a filled polymer. More than one discrete voltage reference plane structure may be employed, for example, when the package is of an LOC configuration with two rows of leads, each having a voltage reference plane secured thereto, or a single voltage reference plane including major portions adhered to leads and interposed connection portions may be applied to all of the leads of an assembly.

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